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EXAMINER
BEREZNY, NEAL

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Please find below and/or attached an Office communication concerning this application or proceeding.

Pursuant to the Remand under 37 CFR 1.193(b)(1) by the Board of Patent Appeals and Interferences on November 30, 2004, that "An examiner's answer should not refer, either directly or indirectly, to more than one prior Office action" a supplemental Examiner's Answer is set forth below:

In order to comply with the above referenced Remand, all references to the statement of the grounds of rejection in previous Office actions have been deleted from the Examiner's Answer, Paper No. 17, filed September 17, 2002.

Supervisory Patent Examiner
Technology Center 2800

Attachment: corrected Examiner's Answer per Remand of 11/30/2004

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 17

Application Number: 09/176,422
Filing Date: October 21, 1998
Appellant(s): WILK ET AL.

David Denker
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/2/01 and supplemental appeal brief filed 9/12/01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

Please note that applicant's ordering of issues in the second supplemental appeal brief, dated 5/15/02, is not consistent with the ordering of issues in the original appeal brief, dated 4/2/01. The second supplemental appeal brief replaces the first supplemental appeal brief, dated 9/5/01, but the original appeal brief was not replaced. The examiner will address the original appeal brief issues first and then the new issues raised in the first and second supplemental appeal briefs. This ordering of issues is preferred, primarily because estoppel issues occurring in the original appeal brief became the basis for later rejections, and then later, new issues of the supplemental

appeal briefs. Therefore, the new issues naturally follow from the original issues. The reverse order would only serve to further confuse the issues.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-25 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,294,571	Fujishiro et al.	3-1994
5,275,687	Choquette et al.	1-1994
5,194,397	Cook et al.	3-1993
4,604,304	Faraone et al.	8-1986
4,851,370	Doklan et al.	7-1989
6,020,247	Wilk et al.	7-1997

Nayar, V. et al., "Atmospheric Pressure, Low Temperature (<500 C) UV/Ozone Oxidation of Silicon", Electronics Letters, vol. 26, no. 3 (Feb. 1, 1990), pp. 205-206.

Wolf, S., "Silicon Processing for the VLSI Era", Vol. 3, Lattice Press, Sunset Beach, Ca., 1995, pp.422-423.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Please note that applicant's ordering of issues in the second supplemental appeal brief, dated 5/15/02, is not consistent with the ordering of issues in the original appeal brief,

dated 4/2/01. The second supplemental appeal brief replaces the first supplemental appeal brief, dated 9/5/01, but the original appeal brief was not replaced. The examiner will address the original appeal brief issues first and then the new issues raised in the first and second supplemental appeal briefs. This ordering of issues is preferred, primarily because estoppel issues occurring in the original appeal brief became the basis for later rejections, and then, later new issues of the supplemental appeal briefs. Therefore, the new issues naturally follow from the original issues.

ORIGINAL ISSUE # 1 – Supplemental ISSUE # 5

oc 12/20/04

~~Claim 18 is rejected under 35 U.S.C. 103(a). This rejection is set forth in prior Office Action, Paper No. 7 & 12, and reiterated here for the Board's convenience.~~

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro et al. (5,294,571) in combination with Nayar et al. (Electronic Letters, 2/1/90, vol.26, no.3). Fujishiro teaches forming a partially completed integrated circuit (IC), fig.2, el.1 and 9, where the substrate surface is cleaned, col.7, ln.8-12, and then exposed in an ozone ambient, col.4, ln.65-67, to form a gate oxide, el.6, and then forming a gate electrode over the gate oxide, el.7. Fujishiro fails to teach conducting the oxide growth at a stable temperature below 200 ^{0}C. Nayar anticipates growing an ultra-thin gate oxide, by UV formed ozone ambient, for microelectronic use, p.206, bottom of first col., after a surface cleaning. Nayar teaches using various stable temperatures, see fig.2, during exposure to an ozone ambient to obtain a thin high-grade oxide. It would be obvious to one of ordinary skill in the art to combine the teachings of Nayar with

Fujishiro to form a low temperature gate oxide in Fujishiro's transistor by using stable temperatures, to form oxides of stable uniform thickness. Nayar provides the motivation to combine on page 205, col.1, start of paper, by pointing out the need to reduce the thermal budget, while maintaining control of the oxide growth rate, so as to avoid associated problems, such as wafer warpage and defect generation.

ORIGINAL ISSUE #2 – Supplemental ISSUE #.6

OC 12/20/04

~~Claims 24-25 are rejected under 35 U.S.C. 103(a). This rejection is set forth in prior Office Action, Paper No. 7 and 12, and reiterated here for the Board's convenience.~~

Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro and Nayar as applied to claims 1-13 above, and further in view of Wolf, vol.3, p.422-423. Wolf teaches using a gate oxide in excess of 8 MV/cm, p.422, characteristic #4. It would be obvious to one of ordinary skill in the art to combine Wolf with Fujishiro and Nayar in order to reduce dielectric breakdown of the gate oxide to reduce catastrophic failure of the device.

ORIGINAL ISSUE #3 – Supplemental ISSUE # 7

OC 12/20/04

~~Claims 1-13 are rejected under 35 U.S.C. 103(a). This rejection is set forth in prior Office Action, Paper No. 7 and 12, and reiterated here for the Board's convenience.~~

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro and Nayar as applied to claim 18 above, and in view of Choquette et al. (5,275,687). In addition to the teaching described above Nayar also teaches the conversion of molecular oxygen to ozone with the use of UV light, see p.205, col.2, first two chemical equations. Also taught by Nayar in the same equations is the use of an inert ambient in addition to the ozone. Further, Fujishiro also teaches keeping the ozone plasma not at the Si surface, col.5, ln.28-40.

Fujishiro and Nayar appear not to specifically state that the Si surface should be atomically flat. Choquette teaches a process to create an atomically flat or smooth surface prior to the formation of a high quality epitaxial layer, see abstract. It would be obvious to one of ordinary skill in the art to combine Choquette with Fujishiro and Nayar to form an atomically flat Si surface prior to the formation of a very thin gate oxide layer. One of ordinary skill in the art at the time of the invention would have been motivated to provide an atomically flat surface before forming a gate oxide that is only 2 or 3 atoms thick. Clearly a surface with deviations greater than 1 or 2 atoms thick would increase the likelihood of defects in the gate oxide resulting in an increase in the leakage current across the gate oxide layer.

ORIGINAL ISSUE # 4 – Supplemental ISSUE # 8

~~Claim 23 is rejected under 35 U.S.C. 103(a). This rejection is set forth in prior Office Action, Paper No. 7 and 12, and reiterated here for the Board's convenience.~~

OC
12/20/04

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishiro, Nayar, and Choquette as applied to claims 1-13 above, and further in view of Wolf, vol.3, p.422-423. Wolf teaches using a gate oxide in excess of 8 MV/cm, p.422, characteristic #4. It would be obvious to one of ordinary skill in the art to combine Wolf with Fujishiro, Nayar, and Choquette in order to reduce dielectric breakdown of the gate oxide to reduce catastrophic failure of the device.

SUPPLEMENTAL NEW ISSUE # 1

Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph. This rejection is set forth in prior Office Action, Paper No. 12, after the appeal brief and before the supplemental appeal brief. The rejection is reiterated here for the Board's convenience.

Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims 1 and 18 contain the limitation, "creating a first uniformly thick, gate oxide film". In appellant's appeal, p.8, ln.3-6, appellant's representative admits that ordinary artisans would not succeed in using Nayar to produce a uniformly thick gate oxide. Since the Nayar process is identical to the claimed process, allegedly with the exception of forming a uniformly thick gate oxide, the disclosure fails to enable one of ordinary skill to produce the claimed limitation of a uniform gate oxide from the claimed process. Appellant need not enable every element of the claims if the element is admittedly well known in the art and would

be obvious to one of ordinary skill in the art at the time of the invention. However, if such an element is critical and the basis of patentability, then appellant would be estopped from asserting that the element is both non-obvious, with regard to patentability, and also obvious, with regard to disclosure, and need not be fully disclosed.

SUPPLEMENTAL NEW ISSUE # 2

Claims 1-17 and 23 were rejected under 35 U.S.C. 112, first paragraph. This rejection is set forth in prior Office Action, Paper No. 12, after the appeal brief and before the supplemental appeal brief. The rejection is reiterated here for the Board's convenience.

Claims 1-17, and 23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claim 1 contains the limitation of providing a substrate with a "clean atomically flat, silicon surface". Appellant's representative admits that ordinary artisans would not expect to be able to form a Silicon substrate that is atomically flat, see appeal, p.6, ln.25-28, yet nowhere in the specifications does appellant teach how one of ordinary skill in the art would be able to obtain an atomically flat Si substrate. Appellant need not enable every element of the claims if the element is admittedly well known in the art and would be obvious to one of ordinary skill in the art at the time of the invention. However, if such an element is

critical and the basis of patentability, then appellant would be estopped from asserting that the element is both non-obvious, with regard to patentability, and also obvious, with regard to disclosure, and need not be fully disclosed.

SUPPLEMENTAL NEW ISSUE # 3

Claims 23-25 are rejected under 35 U.S.C. 112, first paragraph. This rejection is set forth in prior Office Action, Paper No. 12, after the appeal brief and before the supplemental appeal brief. The rejection is reiterated here for the Board's convenience.

Claims 23-25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In each of the claims, 23-25, a limitation is asserted that the claimed process produces breakdown voltages greater than 10 MV/cm or 12 MV/cm. Appellant's admit that a process that used the steps in the claim to make a gate oxide with a breakdown strength of 8 MV/cm would infringe on claim 18 but not claim 24, see appeal p.5, ln.25-28. But neither the claims nor the specifications disclose any process variations that would enable one of ordinary skill in the art to achieve any deviation or control of breakdown voltages. Further, appellant's representative admits that Nayar does not suggest to an ordinary artisan a means of producing breakdown voltages greater than 10 MV/cm or 12 MV/cm, see appeal p.6, ln.2-8, but the process taught by Nayar has not been distinguished from the claimed process, except allegedly in terms of the properties of the final oxide product. By

appellant's admission the claimed process is not enabled. Appellant need not enable every element of the claims if the element is admittedly well known in the art and would be obvious to one of ordinary skill in the art at the time of the invention. However, if such an element is critical and the basis of patentability, then appellant would be estopped from asserting that the element is both non-obvious, with regard to patentability, and also obvious, with regard to disclosure, and need not be fully disclosed.

SUPPLEMENTAL NEW ISSUE # 4

Claim 6 is rejected under 35 U.S.C. 112, first paragraph. This rejection is set forth in prior Office Action, Paper No. 12, after the appeal brief and before the supplemental appeal brief. The rejection is reiterated here for the Board's convenience.

Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Appellants state that the Nayar article teaches a UV/ozone method and that one of ordinary skill in the art would not be able to use the Nayar method to produce the claimed limitation of "at least part of the atmosphere that does not contact the silicon surface includes an ozone plasma", see appeal, p.7, ln.13-17. Neither the claims nor the specifications differentiate between any alleged differences between the prior art and the claimed invention, thereby not enabling one of ordinary skill in the art, by appellant's own admission. Appellant need not enable every element

of the claims if the element is admittedly well known in the art and would be obvious to one of ordinary skill in the art at the time of the invention. However, if such an element is critical and the basis of patentability, then appellant would be estopped from asserting that the element is both non-obvious, with regard to patentability, and also obvious, with regard to disclosure, and need not be fully disclosed.

(11) Response to Argument

ORIGINAL ISSUE # 1 – Supplemental ISSUE # 5

Fujishiro '571 in combination with the Nayar article render claim 18 obvious.

Response to appellant's Original A arguments – Supplement G arguments

Appellant misinterpreted both the Nayar article and the Wolf textbook.

1. Appellant's arguments are based on a serious misreading of both the Nayar article and the Wolf textbook cited in appellant's arguments. The central theme of the Nayar article is **not** the teaching of a "useful method of forming **extremely thick** oxide layers at low temperatures", as stated on line 4, page 5 of the original appeal brief, and line 27 of page 9 of the second supplemental appeal brief. Rather, Nayar teaches a method of growing **ultra-thin** oxide layers, as stated in both the abstract and conclusive paragraphs of the article, which are replicated here for convenience.

> "We report here a new and simple growth technology which is capable of producing **ultra-thin oxides** (=40 Angstroms) on silicon at temperatures below 500C."

"In conclusion, we have demonstrated for the first time the growth of **ultra-thin oxides** by the UV/ozone technique. Initial results suggest that this may form the basis of growing **high quality oxides** for **microelectronic** use."

2. The distinction between thick oxides and high quality ultra-thin oxides in microelectronic use is important because they have very different intended uses. There is a long felt need for ultra-thin gate oxides of high quality for use in microelectronics. An entire field of science has evolved, which is devoted to forming high quality thin oxides, less than 700 angstroms, for use as gate oxides, which are critical to MOSFET performance and functionality, see Wolf, page 422. Whereas, thick oxides, typically 8,000 to 10,000 angstroms, are devoted to isolation uses, such as field oxides, used to electrically isolate entire devices from each other, and interdielectric oxides, used to isolate interconnects, connections between large numbers of MOSFETS, see Wolf, page 337. The standards for thin oxides, due to their applications as gate oxides have standards much different than that for thick oxides. The discussions in Nayar are clearly directed to the "state of the art" standards for ultra-thin oxides and therefore, for gate oxides, and not for thick oxides. The Nayar process is reported to produce oxides less than about 40 angstroms, see fig.2, which are clearly very desirable for thin gate oxides, but not useable nor practical for thick isolation oxide applications. Using a thin oxide for isolation purposed would result in huge capacitances, formidable cross-talk problems, and huge parasitic leakage currents, all of which would conspire to seriously deteriorate the device to the point of non-function. Nayar in the next to last paragraph

on page 206, which is repeated below, clearly states Nayar's expectation of success and provides several suggestions to produce a "state of the art" gate oxide.

> "While these are by no means 'state of the art', these properties are nevertheless **extremely promising** considering that in these initial studies we have not optimized the preparation (no surface preclean was carried out) and growth process. By improving the general processing environment and applying a short post oxidation thermal anneal it should be possible to obtain substantially better breakdown fields, while still minimizing the thermal budget."

3. Further, appellant cites and relies on the Wolf textbook to compare oxide properties reported by the Nayar article with desired properties listed in Wolf, page 422. Appellant's interpretation of the Wolf textbook is incomplete and taken out of context. Appellant fails to recognize that the gate oxide properties listed in Wolf are "**desired**" properties for future "state of the art" gate oxides of future MOS devices, and not the gate oxide properties found in typical ordinary MOS devices at the time of the invention. The properties of typical prior art gate oxides are better exemplified on page 448 of Wolf, which teaches that device failures occur when the breakdown voltage falls below 1MV/cm, and is attributed to pinhole type defects. Other types of defects will occur in the range from 2-6 MV/cm, and others around 3MV/cm. Clearly, Nayar's reported breakdown voltage of 4MV/cm appears to result in absolute predictability of the process to produce useable gate oxides, which may not be "state of the art", but most certainly

demonstrates a reasonable expectation of success. See also In Re Clinton, 188 USPQ 365 (CCPA, 1976).

Nayar oxide used as MOS gate oxide for HFCV test, measures gate oxide performance.

4. Appellant asserts that the Nayar oxide has high fixed charges and therefore could not be used as a **conventional** gate oxide. The Board's attention is directed to Nayar, fig.3, and the paragraph surrounding the figure. The following material is repeated for the Board's convenience.

> "To study the electronic properties of the oxides, high frequency capacitance-voltage (HFCV at 1 MHz), measurements were made on **MOS structures** formed using Al gate contacts."
>
> "The fixed oxide charges (and therefore flatband voltage) are high, but this is **not unusual** for very thin oxides grown at low temperatures. Even the rapid thermal thin oxides grown by Nulman et al. at 1100 ^{0}C have fixed oxide charges in the high $10^{11}/cm^{2}$ range."

5. For the benefit of the Board and appellant, the HFCV test referred to in the above passage is an extremely well known test to anyone of ordinary skill in the art. Its purpose is to test and measure the electronic properties of **gate oxides** for MOS devices used in microelectronics. The test involves building the gate capacitor part of a basic MOS device, in which, the oxide being tested is deposited and used as a **gate**

oxide in the gate capacitor part of an **MOS structure**. The gate electrode is formed with Al contacts over the gate oxide. High frequencies are used to reflect the high switching speeds of the MOS device within a circuit. Deviations from the ideal HFCV curve identify properties and defects in the gate oxide relative to a theoretically ideal gate oxide. For example, fixed oxide charges at the silicon/gate oxide interface will change the curve, and mobile charges will shift the curve and change the forward bias voltage; further discussions could be found in Wolf, vol.1, page 225-228. These properties are directly associated with gate oxides, further supporting Nayar's anticipation of using Nayar's ultra-thin oxide for a gate oxide to be used in microelectronics.

6. In any event, the Nayar article not only anticipates using their oxide as a gate oxide, but they actually build and test the oxide as a gate oxide for use in an MOS structure. Further, Nayar's comparison with Nulman as being of comparable quality, suggests that the Nayar oxide is perhaps not ideal nor 'state of the art', but obviousness does not require absolute predictability in producing ideal or 'state of the art' performance, see *In Re Clinton,* 188 USPQ 365 (CCPA, 1976). Clearly, Nayar anticipated using the ultra-thin oxide as a gate oxide in a MOS device. The identification of less than ideal performance does not negate Nayar's anticipated use of the Nayar process to produce a **high quality ultra-thin oxide** to be used as a gate oxide in **microelectronics.**

Appellant's uniformity arguments exceed the claimed invention

7. Appellant in the original appeal brief, page 4, line 20, and in the second supplemental appeal brief, page 9, line 16, asserts that Nayar does **not mention** that the oxide is **highly** uniform, and therefore concludes that ordinary artisans would not be **assured** that the Nayar oxide had sufficient thickness uniformity for a conventional gate oxide. Appellant also asserts that Nayar's oxide is not uniform because for the **250 ^{0}C** curve of fig.2, second curve from the bottom, there is some scatter in the thickness data. But appellant's claimed invention is directed to a process having the limitation of "a first, uniformly thick, gate oxide", without any mention in the claim of the oxide being **highly** uniform. Using appellant's reasoning, are we to infer that appellant's claimed invention also has no reasonable expectation of success, since the claimed gate oxide is not required to be **highly uniform**? Furthermore, the claimed process is conducted at a temperature **less than 200 ^{0}C**, and not **250 ^{0}C**, as argued. Clearly, appellant is arguing issues not within the scope of the claim. Furthermore, the data for the **150 ^{0}C** curve of fig.2, bottom curve, shows no sign of scatter. Again by applying appellant's own reasoning, the **150 ^{0}C** curve or the Nayar article suggests that their gate oxide has uniform thickness at temperatures below 200 ^{0}C. The Board's attention is directed to Fig.3 of Nayar and the discussion in paragraphs 4-6 above, in which Nayar builds and tests their gate oxide. It is well known in the art, as evidenced in Wolf, p.422, that a uniform gate oxide is required. If Nayar's gate oxide was not uniform then it would be evident in the HFCV plot of fig.3.

8. Appellant's assertion that the Nayar article does not specifically state that their oxide is to be used as a gate oxide is misleading because the entire article is replete with evidence and/or discussions that anyone skilled in the art would understand to be related to gate oxides. In the art, discussions of high quality thin oxides are synonymous with its use as a gate oxide. Appellant's conclusion that a gate oxide must achieve all of the ideal properties in Wolf, page 422, in order for any MOS device to "have a reasonable expectation of success" is ludicrous, since our world is full of functioning MOS devices all having gate oxides with properties falling far short of satisfying all, or even most, of the ideal properties anticipated in Wolf.

Response to Appellant's Original B argument – Supplemental H argument.

Appellant argues more than claimed and has misread Nayar

9. The claimed invention does not contain a limitation requiring **high** thickness uniformity, nor a uniformity <3%. Further, as discussed earlier, see paragraphs 1 and 2, the Nayar article does not teach a "useful method of forming extremely **thick** oxide layers", but rather a useful method of forming an ultra-thin gate oxide, see paragraphs 3-6. Appellant agrees that a uniformly thick oxide would be an inherent property of a gate oxide, see the original appeal brief, page 5, lines 10-11, second supplemental appeal brief, page 10, lines 5-6. Appellant's disagreement with examiner is based on appellant's erroneous assertion that the Nayar article forms a non-gate thick oxide, which examiner addressed in paragraphs 1-6. Examiner further

supports the obviousness of a uniform gate oxide in the Nayar article in the previous discussion of paragraph 7.

ORIGINAL ISSSUE # 2 – SUPPLEMENTAL ISSUE # 6

Fujishiro '571, the Nayar article, and Wolf textbook render claims 24 & 25 obvious.

Response to appellant's Original C arguments – Supplemental I arguments

Appellant argues claim objections, which is not appealable.

10. Appellant's arguments are moot and will not be addressed here because they relate to the Examiner's objection to claims 24-25, which is not an appealable issue.

Response to appellant's Original D arguments – Supplemental J arguments

The Fujishiro, Nayar, and Wolf combination anticipate claims 24 and 25 as obvious.

11. Claims 24 and 25 do not actually further limit the parent claim because the alleged limitation does not limit the claimed process, but rather is an observed resulting property of the process. The appellant asserts that the claimed process produces a gate oxide having breakdown voltages greater than 10 MV/cm and 12 MV/cm. If this assertion is true, then one of ordinary skill in the art, without undue experimentation, should be able to practice the claimed process and achieve these breakdown voltages. Therefore, it should be obvious to an ordinary artisan to achieve these breakdown voltages equally from either the appellant's claimed process or the equivalent combination process of Fujishiro, Nayar, and Wolf, since both processes are identical with respect to the claims. If appellant's assertion is correct that the combined process

could not achieve the higher breakdown voltages, then appellant is neither claiming nor disclosing the critical aspects of their invention.

12. Applicant's attack of the Nayar article, as not reporting the higher claimed breakdown voltages, is irrelevant because as appellant has asserted that with variations on the Nayar process, **"it is not surprising that the results achieved differ"**, see supplemental appeal brief, page 6, lines 7-9. Therefore, it is reasonable to expect that it would be obvious to achieve the higher claimed breakdown voltages with the combined modified Nayar process, which is identical to the **claimed** process.

13. Examiner will elaborate on the method of measuring breakdown voltages to better define the issue. The oxide being measured is placed between two conductors and the voltage is increased until the leakage current between the two conductors reaches a certain value, which is suppose to be when the oxide breaks down and is no longer effective as in insulator. The breakdown voltage is then calculated as the voltage reached, at the established leakage current, divided by the thickness of the oxide being measured. Often artisans will select a lower leakage current threshold than the catastrophic failure threshold, primarily because the device will malfunction or perform poorly long before the oxide actually fails. Clearly, employing a higher leakage current threshold would result in a significantly higher breakdown voltage. It appears that Nayar article used a much lower leakage current threshold than the catastrophic failure

current. The relevant sentence in Nayar on page 206, next to last paragraph, is repeated here:

"The typical breakdown field is approximately 4 MV/cm (assuming breakdown when 10^{-4} A/m^2 is flowing)."

14. Nayar's reported breakdown voltage is based on measuring the voltage when the leakage current reaches 10^{-4} A/m^2, which is very low, only about 10^{-5} pA for a typical MOS device. Typical currents in MOS devices are on the order of 10^{+2} pA. Allowing for typically higher leakage currents would result in significantly higher breakdown voltages, raising Nayar's reported breakdown voltage. Since the examiner is required to interpret the claims as broadly as reasonably possible, it is reasonable that the breakdown voltages claimed by appellant would be the result of catastrophic oxide failure, especially since appellant has failed disclose any teaching as to how appellant has made such measurements. One can establish a lower limit to Nayar's breakdown voltage by referring to the HFCV plot of figure 3 in Nayar. Nayar's oxide is used as a gate oxide in a MOS structure for a HFCV test. Clearly, the CV plot demonstrates a working and functioning MOS device, and therefore, the leakage current experienced in the fig.3 test has not been severe enough to prevent the MOS device from functioning properly, ie. catastrophic failure has not been achieved in the voltage ranges used in the test. Using these voltage ranges to determine a lower limit for the breakdown voltage of Nayar's oxide, we divide the maximum voltage applied to the oxide, 6 volts, by the

thickness of the gate oxide, D_{ox} = 40 angstroms. The following calculation results in a breakdown voltage of **15 MV/cm**, which is only a lower limit.

$$\text{Breakdown Voltage} = \frac{6 \text{ Volts}}{40 \text{ angstroms}} \times \frac{10^{+8} \text{ angstroms}}{\text{cm}} \times \frac{\text{MV}}{10^{+6} \text{ Volts}} = \frac{15 \text{ MV}}{\text{cm}}$$

15. The Nayar article provides data that indicates that under the broader criteria for measuring the breakdown voltage of an oxide, Nayar will meet or exceed 15 MV/cm. Aside from this, since Nayar duplicates the claimed gate oxide growth process and Fujishiro details the steps used to making the MOS device claimed, there is no significant difference between the claimed invention and the combined teachings of Nayar, Fujishiro, and Wolf to account for the alleged differences in the results achieved. Appellant has failed to provide any evidence that at the time of the invention appellant was in possession of a process that would produce results significantly superior to Nayar's oxide as modified by the combination.

ORIGINAL ISSUE # 3 – SUPPLEMENTAL ISSUE # 7

Fujishiro '571, the Nayar article, and Choquette '687 render claim 1 obvious.

Response to appellant's Original E arguments – Supplemental K argument.

16. Appellant relies on the same arguments made for claim 18, Original Issue # 1, which are also applied to claim 1. Examiner also relies on the same response made in Original Issue # 1, paragraphs 1-9, in response to appellant's original E argument.

Response to appellant's Original F arguments – Supplemental L argument.

17. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellant appears to be arguing that since Choquette teaches a method of removing contaminants, including Si, from the surface of a GaAs surface, it would not be obvious to use the Choquette process to form a clean atomically smooth surface prior to growing the gate oxide of Nayar. Further, appellant asserts that there is an absence of a need for a clean atomically flat surface prior to growing an ultra-thin gate oxide, and would therefore, not be obvious. The Board's attention is directed to the abstract of Choquette, col.1, lines 30-34, and col.2, lines 11-14, of Choquette, as well as, the next to last paragraph of Nayar, all duplicated here for the Board's convenience.

> "The **semiconductor** surface thus processed is **atomically smooth** and sufficiently **clean** to permit regrowth of a high quality epitaxial layer."

> "Silicon is a common element and is often found as a surface impurity. Silicon contamination arises, for example, from ion sputtering of quartz liners in ECR plasma sources and from $SiCl_4$ etching gas."

"As shown in Fig.2 workpiece 10 can include a masking layer 11 of **non-III-V** material, such as **silicon oxide**, exposing only a predetermined surface area 12 of the semiconductor layer 13."

"While these are by no means 'state of the art', these properties are nevertheless extremely promising considering that in these **initial studies** we have **not optimized the preparation (no surface preclean** was carried out) and growth process. By **improving the general processing environment** and applying a short post oxidation thermal anneal it should be possible to obtain **substantially** better breakdown fields, while still minimizing the thermal budget."

18. Choquette is used to teach a method of cleaning and providing an atomically smooth semiconductor surface. There is nothing to preclude using the Choquette process on a silicon semiconductor instead of a III-V semiconductor. Appellant's reasoning related to removing Si from a GaAs surface as evidence of non-obviousness is unclear because Si dust, particles, and contaminants are equally problematic to Si semiconductor surfaces, as well. The ideal clean requires the elimination of everything not fully integrated into the single crystal structure, including Si contaminants on the surface of the crystal structure, but not fully integrated into the crystal. As stated in the final rejection, Nayar's gate oxide is as thin as only 2-3 atoms, and deviations greater than 1 or 2 atoms, including Silicon particles and contaminants, would likely act as an undesirable nucleation site and cause a defect, such as a pinhole, in the gate oxide and

degrade the MOS device. Further, appellant's assertion that a need for a clean, atomically smooth surface, is absent and non-obvious, is incorrect. Nayar clearly anticipates the need for a surface preparation, by identifing that surface preparations, such as cleanings, would **substantially** improve the gate oxide's performance.

Claim 6 limitations do not overcome the combined references

Response to appellant's Original G argument – supplemental M argument.

19. Appellant argues that Nayar does not teach a remote ozone plasma. Appellant is attacking the references individually when the rejection is based on the combination of the references. Further, claim 6 does not contain the limitation of a remote ozone plasma. Instead, claim 6 contains the limitation that at least part of the atmosphere, which contains an ozone plasma, is not contacting the surface. This is not the same as an ozone plasma atmosphere **not contacting** the surface. Further, it is inherent that any atmosphere will have at least part of the atmosphere not contacting the surface, only a very thin mono-atomic layer will actually contact the surface.

20. Examiner is required to interpret the claims as broadly as possible, and the term ozone plasma is interpreted as a plasma containing ozone. In Nayar, page 205, col.2, end of the first paragraph, which is repeated below, teaches a **gaseous** atmosphere of ozone and O radicals. A plasma is merely a collection of **charged gas** particles, such as O radicals. Further, Fujishiro, col.5, lines 28-40, teach generating the ozone, ie. ozone plasma, remotely.

"Thus a dynamic equilibrium forms with a reservoir of reactive oxygen species in the form of O_3 and **O radicals**."

ORIGINAL ISSUE # 4 – SUPPLEMENTAL ISSUE # 8

Fujishiro, Nayar, Choquette, and the Wolf text render claim 23 obvious

Response to appellant's Original H argument – Supplemental N argument

21. Appellant assert that claim 23 is patentable because it depends on allegedly allowable base claims. Appellant refers to arguments for claims 18, 24, and 1 above. Examiner also refers to the examiner's answers to those argument for claims 18, 24, and 1.

SUPPLEMENTAL NEW ISSUE # 1

Claims 1-25 stand rejected under 35 USC 112, paragraph 1.

Response to Supplemental A, B, and C arguments

22. The alleged limitation of forming a **uniformly** thick oxide does not actually further limit the claimed process, because it is an **observed** property of the **product** of the claimed **process**. The appellant asserts that claimed process produces a gate oxide that is uniformly thick. If this assertion is true, then one of ordinary skill in the art, without undue experimentation, should be able to practice the claimed process and achieve a uniformly thick oxide. Therefore, it should be equally obvious to an ordinary artisan to achieve a uniformly thick oxide, equally from either the appellant's claimed

process or from the combined process of Fujishiro, Nayar, and/or Choquette, since both processes are identical with respect to the claims. If appellant's assertion is correct, then the combined process should achieve a uniformly thick oxide, but appellant states "it forms oxide films that are **not suitable** for use as gate oxides" and that "there is no evidence that the cited references teach how to achieve a critical limitation of the claim", supplemental appeal, page 10, lines 5-9. The said critical limitation refers to a uniformly thick oxide. Since both the claims and the combined references teach identical processes, appellant's assertions are either incorrect or appellant's claims and specifications fail to claim or disclose the critical aspects of their invention. Further, appellant's usage of **uniform** is vague and indefinite, requiring one to speculate on the alleged differences in processes that would result in an "acceptable" level of uniformity in the gate oxide, which is vague and indefinite. One skilled in the art would not know how to achieve an acceptable level of uniformity, which is vaguely claimed, following seemingly identical processes, if one was to believe that one process produced a high quality gate oxide while the other identical process produced a completely useless gate oxide. Appellant is either committing estoppel, ie. applying a double standard of obviousness, or is not disclosing the critical **process** limitations responsible for such allegedly vastly different results.

SUPPLEMENTAL ISSUE # 2

Rejection of Claims 1-17 and 23 under 35 USC 112, paragraph 1, is withdrawn.

Response to appellant's Supplemental D argument.

23. Examiner withdraws the rejection in light of the Wilk reference having been incorporated into the specifications.

SUPPLEMENTAL ISSUE # 3

Rejection of Claims 24 and 25 under 35 USC 112, paragraph 1, is maintained.

Response to appellant's Supplemental E argument.

24. Claims 24 and 25 do not actually further limit the parent claim because the alleged limitation does not limit the claimed process, but rather is an observed resulting property of any process. The appellant asserts that the claimed process produces a gate oxide having breakdown voltages greater than 10 MV/cm and 12 MV/cm. If this assertion is true, then one of ordinary skill in the art, without undue experimentation, should be able to practice the claimed process and achieve these breakdown voltages. Therefore, it should be obvious to an ordinary artisan to achieve these breakdown voltages, equally, from either the appellant's claimed process or the equivalent combination process of Fujishiro, Nayar, and Wolf, since both processes are identical with respect to the claims. If appellant's assertion is correct that the combined process could not achieve the higher breakdown voltages, then appellant is either committing estoppel, ie. applying a double standard of obviousness, or not claiming nor disclosing the critical aspects of their invention.

25. Applicant states that "the Nayar article that was cited as a similar process does not teach a method **capable** of forming gate oxide films with these breakdown

voltages", see original appeal brief, page 6, lines 3-5, and supplemental brief, page 10, line 26 to page 11, line 1. Examiner has demonstrated that it was obvious and anticipated to modify the Nayar process to include "other structures and surface preparations" as claimed, to produce a process identical with appellant's claimed process, yet appellant insists that such a process is not **capable** of producing a gate oxide with the claimed breakdown voltages. Further, since appellant has failed to define how appellant actually measures the gate oxides breakdown voltage, an ordinary artisan would not be enabled to either practice the claimed invention to achieve a gate oxide with the high breakdown voltages claimed, nor how to even measure the oxide's breakdown voltage. If seemingly identical claimed processes could produce such allegedly varied results, and the means of measuring such results remains unknown, then it would be unclear as to what process and/or oxide did or did not infringe the claims. A skilled artisan trying to duplicate the claimed process would be uncertain as to what process and/or oxide actually satisfied or did not satisfy the claims, and would therefore not be enabled.

SUPPLEMENTAL ISSUE # 4

Rejection of Claim 6 under 35 USC 112, paragraph 1, is withdrawn.

Response to appellant's Supplemental F argument.

23. Examiner withdraws the rejection in light of appellant's arguments and further review of the rejection.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Neal Berezny
July 29, 2002

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